AMENDMENTS TO THE CLAIMS

Claims 1-8 (cancelled)

9. (Currently Amended) A printed wiring board comprising:

(a) a dielectric substrate having upper and lower surfaces;

(b) at least one landless filled plated through hole disposed through the substrate from the upper to the lower surface, the through hole having a first diameter;

(c) the through hole further comprising an inner surface extending from the upper to the lower surface, the inner surface plated with a conductive metal plating, the inner surface plating having an upper end aligned with the substrate upper surface and a lower end aligned with the substrate lower surface;

(d) the through hole filled with a filler composition having upper and surfaces, wherein the filler composition upper surface is aligned with the dielectric substrate upper surface and the through hole inner surface plating upper end, the filler composition upper surface, substrate upper surface and inner surface plating upper end thereby defining a smooth upper subcomposite surface; and

(e) an additively plated unetched first circuitry line having a bottom surface ~~additively~~ plated directly onto the at least one plated through hole inner surface plating upper end and said upper subcomposite surface and thereby electrically connected to said plated through hole, the first circuitry line further comprising a top surface, the first circuitry line bottom surface and first circuitry line top surface ~~said first circuitry further comprising circuit lines~~ having a common line width approximately equal to or less than the first diameter .

10 (Currently Amended) The printed wiring board of claim 9 further comprising a plurality of the first circuitry lines, wherein the plurality of the first circuitry lines further ~~has~~ have an aspect ratio greater than about 0.5.

11. (Previously Amended) The printed wiring board of claim 10 wherein the aspect ratio is greater than about 1.

Claims 12-14 (Cancelled)

15. (Currently Amended) The invention as defined in claim 9 further characterized by a layer of dielectric material disposed on said dielectric substrate and overlying said first circuitry line on said dielectric substrate, said layer of dielectric material having at least one via formed therein.

16. (Currently Amended) The invention as defined in claim 10 further characterized by a layer of dielectric material disposed on said dielectric substrate and overlying said first circuitry line on said dielectric substrate, said layer of dielectric material having at least one via formed therein.

17. (Currently Amended) The invention as defined in claim 11 further characterized by a layer of dielectric material disposed on said dielectric substrate and overlying said first circuitry line on said dielectric substrate, said layer of dielectric material having at least one via formed therein.

18. (Currently Amended) The invention as defined in claim 15 further characterized by a second circuitry disposed on a top surface of said layer of dielectric material and electrically connected to the first circuitry line through the at least one via.

19. (Currently Amended) The invention as defined in claim 16 further characterized by a second circuitry disposed on a top surface of said layer of dielectric material and electrically connected to the first circuitry line through the at least one via.

20. (Currently Amended) The invention as defined in claim 17 further characterized by a second circuitry disposed on a top surface of said layer of dielectric material and electrically connected to the first circuitry line through the at least one via.

21. (Cancelled)

22. (Previously added) The invention as described in claim 9, wherein the filler composition is a thermosetting epoxy resin material comprising electrically conductive metal particulates.

23. (Previously added) The invention as described in claim 10, wherein the filler composition is a thermosetting epoxy resin material comprising electrically conductive metal particulates.

24. (Previously added) The invention as described in claim 11, wherein the filler composition is a thermosetting epoxy resin material comprising electrically conductive metal particulates.

25. (Previously added) The invention as described in claim 9, wherein the inner surface conductive metal plating has a thickness, the thickness from about 0.1 mils to about 4.0 mils.

26. (Previously added) The invention as described in claim 10, wherein the inner surface conductive metal plating has a thickness, the thickness from about 0.1 mils to about 4.0 mils.

27. (Previously added) The invention as described in claim 11, wherein the inner surface conductive metal plating has a thickness, the thickness from about 0.1 mils to about 4.0 mils.

28. (New) A printed wiring board comprising:

(a) a dielectric substrate having upper and lower surfaces;

(b) at least one landless filled plated through hole disposed through the substrate from the upper to the lower surface, the through hole having a first diameter;

(c) the through hole further comprising an inner surface extending from the upper to the lower surface, the inner surface plated with a conductive metal plating, the inner surface plating having an upper end aligned with the substrate upper surface and a lower end aligned with the

substrate lower surface;

(d) the through hole filled with a filler composition having upper and surfaces, wherein the filler composition upper surface is aligned with the dielectric substrate upper surface and the through hole inner surface plating upper end, the filler composition upper surface, substrate upper surface and inner surface plating upper end thereby defining a smooth upper subcomposite surface; and

(e) an additively plated unetched metal pad having a bottom surface plated directly onto the at least one plated through hole inner surface plating upper end and said upper subcomposite surface and thereby electrically connected to said plated through hole, the unetched metal pad further comprising a top surface, the unetched metal pad bottom surface and unetched metal pad top surface having a common pad width approximately equal to the first diameter; and

(f) a first circuitry plated onto the upper subcomposite surface and electrically connected to the unetched metal pad.

29. (New) The printed wiring board of claim 28, wherein the first circuitry comprises an additively plated unetched first circuitry line having a bottom surface plated directly onto the upper subcomposite surface, the first circuitry line further comprising a top surface, the first circuitry line bottom surface and first circuitry line top surface having a common line width.

30. (New) The printed wiring board of claim 29 further comprising a plurality of the first circuitry lines, wherein the plurality of the first circuitry lines further have an aspect ratio greater than about 0.5.

31. (New) The printed wiring board of claim 30 wherein the aspect ratio is greater than about 1.